What is claimed is:

1. An SOI-based electro-optic arrangement comprising

a silicon substrate;

a buried dielectric layer;

a single crystal silicon (SOI) layer disposed over the buried dielectric layer;

at least one optical component area including

a thin dielectric layer disposed over a portion of the SOI layer; and

a silicon layer disposed over the thin dielectric layer so as to overlap in part the SOI layer; and

at least one electrical component area including

a thin dielectric layer disposed over a separate portion of the SOI layer; and

a heavily-doped gate metal-like silicon layer disposed over the thin dielectric layer, wherein one or more optical devices are formed in each of the optical component areas and one or more electrical devices are formed in each of the electrical component areas; and

a common electrical interconnect arrangement including one or more layers of metallization.

2. The SOI-based arrangement as defined in claim 1 wherein the buried dielectric layer comprises silicon dioxide.

3. The SOI-based arrangement as defined in claim 2 wherein the thickness of the silicon dioxide layer is greater than 0.4 μm.

4. The SOI-based arrangement as defined in claim 1 wherein the thickness of the single crystal silicon layer is less than one micron.

5. The SOI-based arrangement as defined in claim 1 wherein the silicon layer in the at least one optical component area has a thickness less than one micron.

6. The SOI-based arrangement as defined in claim 1 wherein the silicon layer in the at least one optical component area has a thickness substantially equal to the thickness of the heavily-doped gate metal-like silicon layer in the at least one electrical component area.

7. The SOI-based arrangement as defined in claim 1 wherein the silicon layer in the at least one optical component area has a thickness less than the thickness of the heavily-doped gate metal-like silicon layer in the at least one electrical component area.

8. The SOI-based arrangement as defined in claim 1 wherein the silicon layer in the at least one optical component area has a thickness greater than the thickness of the heavily-doped gate metal-like silicon layer in the at least one electrical component area.

9. The SOI-based arrangement as defined in claim 1 wherein the thickness of the silicon layer in the at least one optical component area is chosen to confine the optical mode peak intensity to substantially overlap the carrier modulation region.

10. The SOI-based arrangement as defined in claim 1 wherein the thin dielectric layer in the at least one optical component area has a thickness less than 1000 Å.

11. The SOI-based arrangement as defined in claim 1 wherein the thin dielectric layer in the at least one optical component area is chosen from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, bismuth oxide and hafnium oxide.

12. The SOI-based arrangement as defined in claim 1 wherein the thin dielectric layer in the at least one optical component area has a thickness substantially equal to the thickness of the thin dielectric layer in the at least one electrical component area.

13. The SOI-based arrangement as defined in claim 1 wherein the thin dielectric layer in the at least one optical component area has a thickness less than the thickness of the thin dielectric layer in the at least one electrical component area.

14. The SOI-based arrangement as defined in claim 1 wherein the thin dielectric layer in the at least one optical component area has a thickness greater than the thickness of the thin dielectric layer in the at least one electrical component area.

15. The SOI-based arrangement as defined in claim 1 wherein the silicon layer in the at least one optical component area is selected from the group consisting of single crystal silicon, substantially single crystal silicon, strained silicon, amorphous silicon and polysilicon.

16. The SOI-based arrangement as defined in claim 15 wherein the polysilicon is selected from the group consisting of grain-size-enhanced polysilicon, grain-aligned polysilicon, grain-boundary-passivated polysilicon.

17. The SOI-based arrangement as defined in claim 1 wherein the silicon layer in the at least one optical component area comprises a single layer structure.

18. The SOI-based arrangement as defined in claim 1 wherein the silicon layer in the at least one optical component area comprises a multiple layer structure.

19. The SOI-based arrangement as defined in claim 18 wherein the multiple layer structure comprises more than one form of silicon.

20. The SOI-based arrangement as defined in claim 18 wherein each layer of the multiple layer structure comprises the same form of silicon.

21. The SOI-based arrangement as defined in claim 1 wherein at least one corner of the silicon layer in the at last one optical component area is rounded to reduce optical signal loss.

22. The SOI-based arrangement as defined in claim 1 wherein at least a portion of the silicon layer in the at least one optical component area is doped to form an active "semiconductor-like" optical device region.

23. The SOI-based arrangement as defined in claim 22 wherein the portion of the SOI layer within the at least one active optical device region is doped to exhibit a conductivity type opposite to that of the silicon layer.

24. The SOI-based arrangement as defined in claim 22 wherein each doped portion contains separate regions of low dopant concentration, for modulation of an optical signal and separate regions of high dopant concentration, for application of an electrical operating signal.

25. The SOI-based arrangement as defined in claim 1 wherein at least a portion of the silicon layer in the at least one optical component area is undoped to form a passive optical device region.

26. The SOI-based arrangement as defined in claim 1 wherein the common electrical interconnect arrangement comprises silicide contact areas disposed on both selected ones of the optical component areas and the electrical component areas, the silicide contact areas comprising the same material and formed simultaneously to exhibit an essentially equal thickness.

27. The SOI-based arrangement as defined in claim 26 wherein the contact silicide is selected from the group consisting of: tantalum silicide, titanium silicide, tungsten silicide, cobalt silicide, nickel silicide, and molybdenum silicide.

28. The SOI-based arrangement as defined in claim 1 wherein the common electrical interconnect arrangement comprises contact areas connecting silicide to a first metal layer disposed on both the active optical component areas and the electrical

component areas, the contact areas comprising the same material and formed simultaneously.

29. The SOI-based arrangement as defined in claim 1 wherein the common electrical interconnect arrangement comprises at least one layer of metal disposed on both the active optical component areas and the electrical component areas, comprising the same material and formed simultaneously to provide electrical connection between at least one optical device and at least one electrical device.

30. The SOI-based arrangement as defined in claim 1 wherein the common electrical interconnect arrangement comprises at least two layers of metal disposed on both the optical component areas and the electrical component areas interconnected using inter-metal layer connecting vias, comprising the same materials and formed simultaneously.

31. The SOI-based arrangement as defined in claim 1 wherein the minimum distance between any metal layer of the at least one metal layer and a light confining region of the active optical device in the optical area is greater than one micron.

32. The SOI-based arrangement as defined in claim 1 wherein the minimum distance between any silicide layer and a light confining region of the optical device in the optical area is greater than 0.2 micron.

33. The SOI-based arrangement as defined in claim 1 wherein the single crystal silicon layer has an optical defect count of less than a predetermined number of defects/cm^2, a defect being defined as an element exhibiting a dimension of greater than a predetermined fraction of the effective wavelength, $\lambda_{effective}$, of the light traveling in the SOI layer.

34. The SOI-based arrangement as defined in claim 33 wherein the predetermined number of defects is selected from the group consisting of 1 defect/cm^2, 10 defects/cm^2 and 100 defects/cm^2.

35. The SOI-based arrangement as defined in claim 33 wherein the predetermined fraction of $\lambda_{effective}$ is chosen from the group consisting of 1/5, 1/10, 1/15 and 1/20.

36. The SOI-based arrangement as defined in claim 1 wherein the single crystal silicon layer has an optical defect count of less than a predetermined number of defects/cm^2, a defect being defined as an element exhibiting a dimension of greater than a predetermined fraction of the thickness of the SOI layer.

37. The SOI-based arrangement as defined in claim 36 wherein the predetermined number of defects is selected from the group consisting of 1 defect/cm^2, 10 defects/cm^2 and 100 defects/cm^2.

38. The SOI-based arrangement as defined in claim 36 wherein the predetermined fraction of the thickness of the SOI layer is chosen from the group consisting of ½, 1/3, ¼ and 1/5 and 1/10.

39. The SOI-based arrangement as defined in claim 1wherein the optical defect count is reduced by performing a hydrogen anneal operation prior to depositing the relatively thin dielectric layer over the SOI layer.

40. The SOI-based arrangement as defined in claim 1 wherein the combined thickness of the SOI layer, the dielectric layer and the silicon layer in the at least one optical component area is selected to support the propagation of a single optical mode in the vertical direction.

41. The SOI-based arrangement as defined in claim 1 wherein the SOI layer is formed using an epitaxial growth process to reduce the optical defect density.

42. The SOI-based arrangement as defined in claim 1 wherein a window is opened from the top surface of the arrangement to expose a portion of the SOI layer used to form an optical coupling area.

43. The SOI-based arrangement as defined in claim 42 wherein the final surface of the exposed portion of the SOI layer is atomically smooth.

44. The SOI-based arrangement as defined in claim 42 wherein the optical coupling area provides evanescent coupling of optical signals into and out of the SOI layer.

45. The SOI-based arrangement as defined in claim 42 wherein the window is formed using a single photolithography/etch step.

46. The SOI-based arrangement as defined in claim 42 wherein the window is formed using a plurality of photolithography/etch steps.